IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: To Be Assigned
Examiner: To Be Assigned

In re PATENT APPLICATION of

Applicant(s): Yoko KAJITA

Serial No.: To Be Assigned

Filed: Herewith

For: Method Of Manufacturing A Semiconductor Device

Atty. Dkt.: OKI 364

INFORMATION DISCLOSURE STATEMENT

July 31, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(b)(1).

Attached is a copy of one (1) published Japanese patent together with the English-language Abstract, and a copy of an English-language publication. Any relevance of the Japanese patent can be gleaned from the attached English language Abstract and from the present specification, and any relevance of the English-language publication is self-evident. The publications are listed on the attached Form PTO-1449.

Since this Information Disclosure Statement is being filed with the application, no certification or fee is required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to the documents submitted. Consideration of the submitted documents is respectfully requested.

Respectfully submitted,

July 31, 2003
Date

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	Atty. Docket: **OKI 364**	Application No.: **Not yet assigned**
	Applicant: **Kojo KAJITA**	
	Filing Date: **July 31, 2003**	Group Art Unit: **Not yet assigned**

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub-Class	Trans-Lation
	AI	**2001-257357**	**09/21/01**	**Japan**			**Abstract**
	AJ						
	AK						
	AL						
	AM						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	Recessed-Channel Structure for Fabricating Ultrathin SOI MOSFET with Low Series Resistance, Mansun Chan, Fariborz Assaderaghi, Stephen A. Parke, Chenming Hu, *Fellow*, IEEE, and Ping K. Ko, *Senior Member*, IEEE IEEE Electron Device Letter, Vol. 15, No. 1, January 1994

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.